

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re Patent Application of

Atty Dkt. 124-930

WILKINSON et al

C# M#

Serial No. 10/084,652

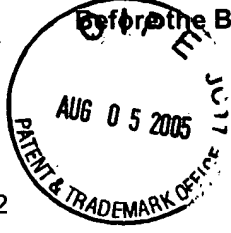
TC/A.U.: 2841

Filed: February 28, 2002

Examiner: T. Phan

Date: August 5, 2005

Title: SPACERS FOR CELLS HAVING SPACED OPPOSED SUBSTRATES



BAF
JFW

Mail Stop Appeal Brief - Patents

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**☐ **NOTICE OF APPEAL**

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences
from the last decision of the Examiner twice/finally rejecting
applicant's claim(s).

\$500.00 (1401)/\$250.00 (2401) \$

☒ An appeal **BRIEF** is attached in the pending appeal of the
above-identified application \$500.00 (1402)/\$250.00 (2402) \$ 500.00

☐ Credit for fees paid in prior appeal without decision on merits -\$ ()

☐ A reply brief is attached. (no fee)

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this
paper and attachment(s)
One Month Extension \$120.00 (1251)/\$60.00 (2251)
Two Month Extensions \$450.00 (1252)/\$225.00 (2252)
Three Month Extensions \$1020.00 (1253)/\$510.00 (2253)
Four Month Extensions \$1590.00 (1254)/\$795.00 (2254) \$

☐ "Small entity" statement attached.

Less month extension previously paid on -\$ ()

TOTAL FEE ENCLOSED \$ 500.00

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension.
The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or
asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this
firm) to our **Account No. 14-1140**. A duplicate copy of this sheet is attached.

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Signature: 



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BRIEF FOR APPELLANT
On Appeal From Final Rejection
From Group Art Unit 2841

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APPEAL BRIEF

Sir:

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, QinetiQ Limited, a United Kingdom corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals related to this subject application. There are no interferences related to this subject application.

III. STATUS OF CLAIMS

Claims 1-34 are pending. Dependent claims 22-27 are indicated as being allowable. Claims 1-21 and 28-34 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent 5,838,414 to Lee et al. in view of U.S. Patent 5,902,165 to Levine.

IV. STATUS OF AMENDMENTS

No after-final amendments have been submitted.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The claimed subject matter relates to active backplanes for use with a spaced opposed front electrode, which can be used in one non-limiting example application in a spatial light modulator formed using a smectic liquid crystal layer disposed between an active semiconductor backplane and a common front electrode. As explained on page 3 of the specification, active backplane devices include a plurality of active electronic elements, such as transistors, for energizing corresponding pixels. Two common forms are thin film transistors on silica/glass backplanes and semiconductor backplanes.

The claimed subject matter is described in the context of the non-limiting , example embodiment set forth in the specification. Figures 1 and 2 show a side and an exploded view respectively of a liquid crystal cell having an active backplane 3 with one surface mounted on a substrate 2. Formed on the other surface is an array of active mirror pixels 4 arranged in columns and rows. Liquid crystal material is injected

between that array 4 on the surface of the backplane 3 and an indium-tin-oxide conductive layer 8 formed on a glass front electrode 7. An aluminum contact 9 provides electrical contact to conductive layer 8 in the assembled cell.

Figure 3 shows the active backplane 3 with the array 4 is surrounded by various row and column drive/scanning circuitry. Figures 6 and 7 show that each active pixel element in array 4 includes an NMOS transistor 52 having a gate 59 connected to one of a set of a row conductors scanned by row scanners 44 and 45, a drain electrode 60 connected to one of a set of column conductors scanned by column scanners 42 and 43, and a source electrode or region 63 (Figure 7) which either is in the form of a pixel mirror electrode 65 (or is connected to a mirror electrode). Together with an opposed portion of the common front electrode 6 and interposed chiral smectic liquid crystal material 20, the rear located mirror electrode forms a liquid crystal pixel cell which has capacitive characteristics.

For smectic liquid crystal material, the thickness the liquid crystal layer in the active backplane can be very small, e.g., on the order of a few microns as compared to 20-100 microns if nematic liquid crystal is used. See pages 2 and 5 of the specification. Such smaller liquid crystal thicknesses have several benefits, but there are associated problems as well. For example, as the liquid crystal thickness approaches dimensions associated with the underlying backplane structure and/or the magnitude of any possible deformation of the liquid crystal cell structure by flexing or other movement of the substrates, there may be less uniformity across the pixel area. There also is the greater possibility for short circuiting across the cell. The alignment in chiral smectic liquid

crystal cells is also mechanically sensitive and can be destroyed by mechanical impulses or shock.

Thus, there is a need for correct and stable spacing between the two substrates of a cell incorporating an active backplane, and this is particularly so in the case of smectic liquid crystal cells that have very thin liquid crystal layers. The inventors conceived of a backplane spacer that would satisfy these criteria and overcome these problems.

Referring to the non-limiting example in Figure 1, insulating spacers 25 are formed on the active backplane 3 and extend up to the front electrode 6 for a predetermined, precise and stable distance from the silicon substrate. Liquid crystal material fills the spaces defined. Advantageously, the spacers 25 on the active backplane 3 are formed on the silicon substrate 2 simultaneously with formation of the electronic elements formed on the active backplane, using all or at least some of the same processing steps.

As shown in Figures 4 to 6, the spacers 25 are in the form of columns of generally square cross-section (e.g., 3 microns by 3 microns). The spacers 25 are integral with the backplane 3 and are distributed over the pixel array—one for each pixel 27. They may be supplemented by spacers 26 distributed in the glue lanes 21, 22 between the pixel array and an out area 22a for the control circuitry (Figure 3) which is coupled to the array.

The electronic array elements shown in Figure 6 include an NMOS transistor 52 and a pixel mirror 53, with the transistor being higher over the backplane. These active electronic elements are formed using a first electronic element layer 57 and a second electronic element layer 58 upon which various electrodes are formed that are part of row and column electrodes.

At the same time that these two electronic element layers are formed, the spacer 25 shown at the left side of Figure 6 is formed in part using the same layers 57 and 58. In the spacer region 25, the first layer 57 is thicker over the backplane as compared to the transistor region and the pixel mirror region. The second layer 58 also rises higher over the backplane in the spacer region 25 as compared to the transistor region and the pixel mirror region. In this example, the spacer 25 includes (moving from top to bottom) a metal layer 68, silicon dioxide layer 58, metal layer 67, silicon dioxide layer 57, polysilicon layers 72 and 70 spaced by a thin oxide layer 71, and a field oxide layer 69 formed in the substrate 51. The metal layers 67 and 68 are of the same material and are deposited at the same time as the electrodes 59 and 60 of the transistor 52. Even though the spacer 25 includes metallic layers, the spacer provides good insulation between the front electrode and active backplane. Ultimately, the spacer 25, which is laterally separated from the electronic elements 52 and 53, rises higher over the backplane than the electronic elements in the array and is insulated from the electronic elements.

By forming insulating spacers in this manner, it is possible to locate them accurately relative to other elements on the backplane, thereby avoiding any interference with optical or electrical properties. And creating them at the same time as the active and electronic elements of the backplane and using the same processes improve efficiency and reduce cost.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The sole rejection to be reviewed on appeal is the obviousness rejection based on the combination of Lee and Levine.

VII. ARGUMENT

A. The Lee Reference Lacks Multiple Claim Features From The Independent Claims

1. Lee Lacks the Claimed Array

Lee teaches a passive matrix liquid crystal device where row and column electrodes are formed on opposing substrates to define a matrix of addressable pixel locations. Drive electronics (e.g. row and column drivers) external to the device are used to apply voltage to the row and column electrodes to produce appropriate voltage levels at a pixel. Passive addressing is described at lines 19-27 of column 1 and lines 47-51 of column 4. The independent claims 1, 4, and 29 on appeal recite an array of electronic elements, e.g., transistors, that make the backplane an active backplane. The differences between active backplane devices and a passive matrix device like that described in Lee are explained in some detail at page 2, line 25 to page 5, line 17 of the present application. Lee's lower substrate 2 and upper substrate 4 each include a single layer of transparent conductive material (typically Indium Tin Oxide, ITO) etched to form lower and upper stripe electrodes, respectively. Electrodes are not electronic elements, and thus, Lee fails to teach a backplane having an array of electronic or electrical elements.

The Examiner is contending that Lee's electrodes 6 correspond to the claimed array of electronic elements. But such a reading is at odds with how a person of ordinary skill in the art would understand the term electrode. An electrode is a conductor or charge collector/emitter rather than an electronic element. Moreover, claims 1 and 4 recite "electronic element layers," and their respective dependent claims 32 and 16 recite the *additional element* of "an electrode." Clearly, an electrode is not the same as the claimed electronic element.

But even if one could take the position that an electrode is the claimed electronic element, which cannot be done for the reasons just explained, Lee's electrodes 6 do not include the claimed "at least a first electronic element layer and a second electronic element layer." The Examiner identifies the upper electrode 8 as one electronic element layer. But how can this be the case since the Examiner is contending that an electrode is a electronic element—not a layer and the lower electrode 6 does not "comprise" the upper electrode? The Examiner identifies the liquid crystal material 22 as the other electronic layer. This reading is also flawed because the liquid crystal material 22 can not reasonably be understood to be a part of the lower electrode 6. The two layers 8 and 22 are simply not electronic element layers; nor do the electrodes 6 in any way "comprise" or include the upper electrodes or the liquid crystal material.

2. Lee Lacks the Claimed Spacer

The Examiner seems to have misunderstood this claim element. Claim 1 recites at least one separate spacer that "comprises at least a first spacer layer and a second spacer layer." The Examiner states that Lee's spacer 18 "rises higher over the back plane

[2] than the array [6] and a second spacer layer [10]." But the Examiner does not identify both the claimed first and second spacer layer. Element 10 in Lee is another spacer completely separate from spacer 18—it is not a layer of spacer 18. Claim 1 does not define a backplane having two different types of spacers. Rather, it defines at least one separate spacer that comprises at least a first spacer layer and a second spacer layer.

The Examiner admits that Lee also fails to teach the claimed feature that the "first electronic element layer is comprised of substantially the same material as said first spacer layer and said second electronic element layer is comprised of substantially the same material as said second spacer layer." So Lee fails to teach virtually every feature recited in claim 1. The Examiner does not even address the feature recited in claim 4 that "the material of said first spacer layer is modified relative to the materials of said first electronic element layer." In claim 29, the Examiner fails to show where Lee discloses "wherein the processes used for making parts of at least one said element are also used simultaneously to form parts of spacers on the backplane laterally spaced from said elements." The office action simply states: " the claimed method steps are necessitated by the product structure." The structure in Lee of two different spacers 18 and 10 does not necessitate forming them as part of forming the lower electrode 6. In fact, the process to form lower electrode 6 is clearly not part of the process to make spacers 18 and 10. Indeed, the electrodes 6 have already been formed by the time the spacer 18 is formed as is evident from Fig. 6 in Lee.

B. Levine Does Not Disclose the Independent Claim Features Missing From Lee

Turning now to Levine, the Examiner asserts that "Levine discloses a plurality of spacers [125] having the same material as the electronic layers." The claims do not recite the spacers having the same material, and the Examiner fails to identify the claimed first and second electronic element layers in Levine. In an attempt to speculate how the Examiner may be reading Levine by following the Examiner's flawed reading of claim 1 onto Lee, the claimed electronic elements would apparently be read by the Examiner onto Levine's cathode electrodes 18. The "insulating spacer" 125 is made of silicon dioxide, and the cathode mesh 18 is a conductor such as niobium, as described in col. 5, lines 45-64. So they are clearly made from different materials. Even the layer 15 on top of the electrodes 18 is pure silicon rather than silicon dioxide. See col. 5, lines 55-57. Indeed, layer 125 is not "substantially similar" to any other layer present in the emitter plate structure. There is simply no mention that layer 125 could be formed from the same material as the other (i.e., electrode, resistive, and SiO) layers.

The field emission device (FED) disclosed in Levine comprises an anode plate 11 that is spaced apart from the emitter plate 110 (see lines 24-26 of column 1, lines 15-16 of column 4, figure 6 of Levine). The insulating spacer 125 does not perform a spacing function between the cathode or emitter plates. The main electronic elements of the FED emitter plate 110 are the array of micro-tip cones 14 that emit the electrons that are accelerated to the anode plate 11. So spacer layer 125 does not "rise higher over the backplane than the array" of electronic elements 14, as recited in claims 1 and 4. In

addition, the spacer layer 125 does not comprise a first spacer layer and a second spacer layer, as recited in claims 1 and 4 because layer 125 is just one layer of one material.

Regarding claim 29, Levine does not teach "wherein the processes used for making parts of at least one said element are also used simultaneously to form parts of spacers on the backplane laterally spaced from said elements." The various layers (including layer 125) used to form the emitter/cathode 110 are successively formed on the glass substrate 20. See lines 40-45 of column 5 of Levine.

Thus, even if the combination of Lee and Levine could properly be made, that combination fails to disclose all the features of the independent claims 1, 4, and 29.

C. The Combination of Lee and Is Based On Improper Hindsight

The Examiner uses improper hindsight to combine Lee and Levine in a failed attempt to show the missing independent claim features. A proper motivation to combine requires an appreciate of the desirability of making the combination. It is not measured by the feasibility of making the combination. See *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 (Fed. Cir. 2000). The Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and no knowledge of the claimed invention, would select the elements from the cited prior art references for the combination in the manner claimed. *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). The Examiner fails to make such a showing in this case. The obviousness rejection is improper on this ground as well.

The Examiner's only justification for the combination is "to facilitate manufacture." But the Examiner fails to explain how. It is not even clear what structures

in Levine would be used in Lee; nor how they would be used. To simply assert a general desired end, like "facilitating manufacture," without explaining how cannot be a legal motivation. The Examiner does not point to any text in either reference that the manufacturing process for spacer 125 even achieves the desired end in Levine itself—let alone in Lee.

In addition, there is no motivation for a person of ordinary skill to combine teachings from such remote technical fields. Lee is from the field of passive matrix LCDs. Levine's field emission devices are completely unrelated to LCD devices. The Examiner's attempt to combine Lee with Levine is at best a hindsight "forced" attempt to reconstruct the claimed subject matter.

D. Dependent Claim Features Are Patentable For Additional Reasons

Claims 2 and 30 recite that the "the backplane is a semiconductor backplane." There is no teaching of a semiconductor backplane in Lee. Lee describes a passively addressed LCD that is formed from two glass substrates that carry electrode layers (e.g. layers of Indium Tin Oxide) and various insulating and alignment layers. There is no mention in Lee of using any semiconductor material whatsoever, let alone using a semiconductor backplane (e.g. a wafer of semiconductor material) to provide the active electronic elements.

Nor does Lee's passive electrode matrix disclose "an active backplane in which the array comprises active electronic elements" as recited in 20. Claim 5 recites: "all the layers in the spacer correspond in material and order to all the layers in said at least one

electrical or electronic element." This feature is not taught by Lee. The spacers 18 are made from a different material from and are formed at a later time than the electrodes 6.

Claim 3 defines that the spacers include at least one additional space layer so that the spacer comprises more than three layers. As noted above, Lee fails to teach a spacer formed from two layers let alone any spacers having more than three layers.

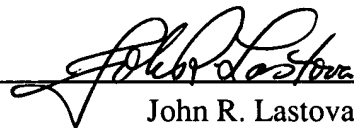
VIII. CONCLUSION

Multiple features of the independent claims are not disclosed or suggested by the combination of Lee and Levine. There is no proper motivation to combine their teachings as the Examiner proposes. Each missing claim feature and the lack of motivation for each combination is an independent ground for reversal. The Board should reverse the outstanding rejections.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____



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JRL/sd
Enclosures
Appendices

IX. CLAIMS APPENDIX

1. A backplane comprising:

an array of electrical or electronic elements, each of said electrical or electronic elements comprising at least a first electronic element layer and a second electronic element layer; and

at least one separate spacer which rises higher over the backplane than said array, said at least one separate spacer comprises at least a first spacer layer and a second spacer layer, wherein said first electronic element layer is comprised of substantially the same material as said first spacer layer and said second electronic element layer is comprised of substantially the same material as said second spacer layer.

2. A backplane according to claim 1 wherein the backplane is a semiconductor backplane.

3. A backplane according to claim 1 wherein said at least one spacer includes at least one additional spacer layer, said at least one additional spacer layer and said first and second spacer layers forming a series of more than two layers.

4. A backplane comprising:

an array of electrical or electronic elements, each of said electrical or electronic elements comprising at least a first electronic element layer and a second electronic element layer; and

at least one separate spacer which rises higher over the backplane than said array, said at least one separate spacer comprises at least a first spacer layer and a second spacer layer, wherein the material of said first spacer layer is modified relative to the material of said first electronic element layer.

5. A backplane according to claim 1 wherein all the layers in the spacer correspond in material and order to all the layers in said at least one electrical or electronic element.

6. A backplane according to claim 1 wherein the spacer is electrically insulating between a top and bottom of said spacer.

7. A backplane according to claim 1 wherein there is a plurality of said spacers distributed over the backplane.

8. A backplane according to claim 7 wherein at least some of the spacers are regularly distributed over the array.

9. A backplane according to claim 7 wherein the array provides a plurality of addressable locations, and each location has at least one said spacer associated therewith.

10. A backplane according to claim 9 wherein each location has only one said spacer associated therewith.

11. A backplane according to claim 7 wherein at least one said spacer is in the form of a column having a generally square cross-section.

12. A backplane according to claim 7 wherein at least one said spacer is in the form of a ridge having an elongate cross-section.

13. A backplane according to claim 1 wherein said array is covered by an insulating layer which also extends over the said spacer or said plurality of spacers.

14. A backplane according to claim 13 wherein said insulating layer has a generally constant thickness.

15. A backplane according to claim 13 wherein the upper surface of said insulating layer is substantially flat.

16. A backplane according to claim 13 wherein an electrode is deposited on said insulating layer and is coupled to a said element of said array.

17. A backplane according to claim 16 wherein said electrode is reflective.

18. A backplane according to claim 17 wherein the reflectivity of the electrode is greater than the reflectivity of conductive layers occurring in the electrical or electronic element and/or spacers of the array.

19. A backplane according to claim 1 wherein the top surface thereof is treated in a manner to induce liquid crystal alignment.

20. A backplane according to claim 1 wherein the backplane is an active backplane in which the array comprises active electronic elements.

21. A backplane according to claim 1 wherein at least some of the spacers are located externally of the array.

28. A method of producing a backplane as defined in claim 1, wherein processes used for making parts of at least one said element are also used simultaneously to form parts of said spacers.

29. A method of producing a backplane having at least one region containing an array of electrical or electronic elements, wherein the processes used for making parts of at least one said element are also used simultaneously to form parts of spacers on the backplane laterally spaced from said elements.

30. A method according to claim 29 wherein said backplane is a semiconductor backplane.

31. A method of producing a backplane according to claim 29 wherein the spacers comprise at least two layers of substantially the same material and occurring in the same order as is found in at least one said electrical or electronic element.

32. A cell comprising a backplane as defined in claim 1 and an opposed electrode sealed thereto in spaced relation.

33. A cell according to claim 32 wherein liquid crystal material is located between the electrode and the backplane.

34. A cell according to claim 33 wherein the liquid crystal material has a smectic phase.

X. EVIDENCE APPENDIX

There is no evidence appendix.

XI. RELATED PROCEEDINGS APPENDIX

There is no related proceedings appendix.